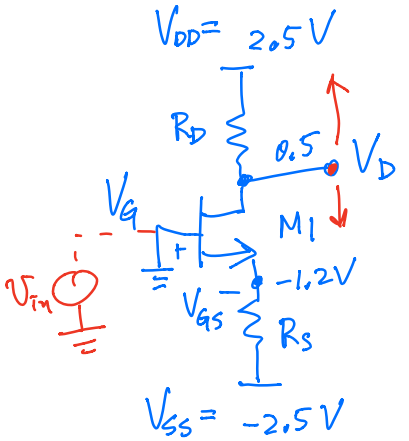


NMOS, $V_{t,n} = 0.7\,V$, $\mu_n C_{ox} = k_n' = 100\,\mu A/V^2$

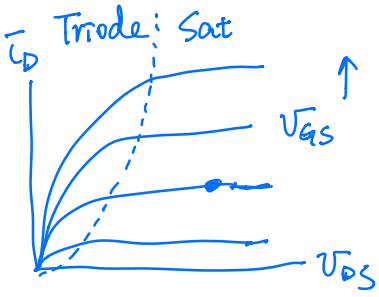
$W/L = 32\,\mu m / 1\,\mu m$

$\Rightarrow k_n = k_n'\left(\frac{W}{L}\right) = 3.2\,mA/V^2$

Assume M_1 is in saturation

$I_D = \frac{1}{2} k_n V_{OV}^2$

Design: → set I_D, V_{DS} (DC)



↳ Amplifier gain $\propto \sqrt{I_D}$

Power consumpt $(V_{DD} - V_{SS}) \times I_D$

V_{DS}: Output swing ↑ Peak-to-peak

Goal: $I_D = 0.4\,mA$, $V_D = 0.5V$

$I_D = \frac{1}{2} k_n V_{OV}^2 = 0.4\,mA = (1.6\,mA/V^2) \cdot V_{OV}^2$

$V_{OV}^2 = \frac{1}{4} \Rightarrow V_{OV} = \frac{1}{2} = 0.5V = V_{GS} - V_{t,n}$

$\Rightarrow V_{GS} = 0.5 + 0.7 = 1.2V = V_G - V_S$ ($V_G = 0$)

$\Rightarrow V_S = -1.2V$

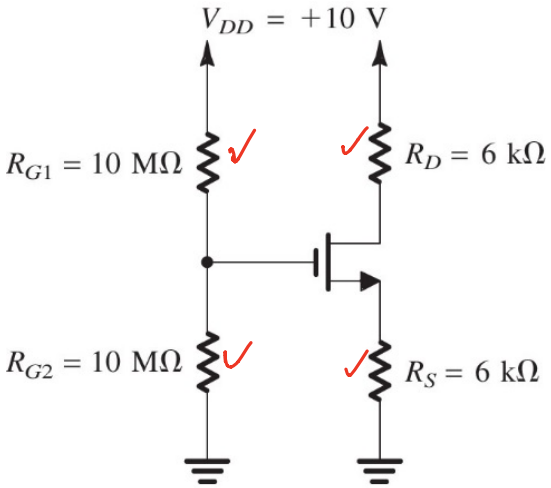
$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(2.5 - 0.5)V}{0.4\,mA} = 5\,k\Omega$

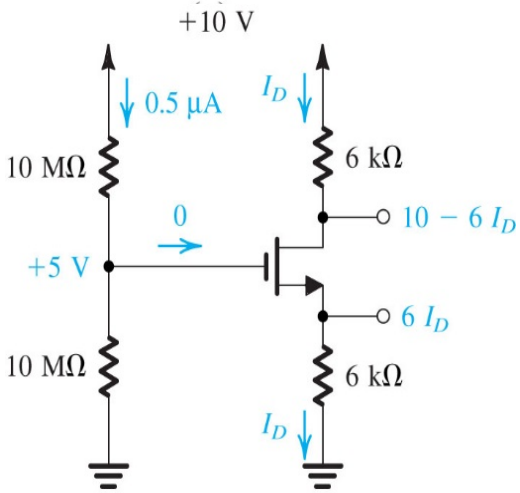
$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{(-1.2 - (-2.5))V}{0.4\,mA} = \frac{1.3}{0.4} = 3.25\,k\Omega$ #

$V_{DS} = V_D - V_S = 0.5 - (-1.2) = 1.7V > V_{OV} = 0.5V$

Assumption is valid #

Example Circuit (2)





(b)

The resistor divider is a common bias circuit.

To solve the DC bias condition, it means to solve I_D, V_{DS}, V_{GS}

The NMOS has $V_{tn} = 1V$, $k_n = \mu_n C_{ox} \frac{W}{L} = 1mA/V^2$

First, solve $V_G = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}} = 10 \frac{5}{5+5} = 5V$

$V_{GS} = 5 - I_D R_S = 5 - 6I_D$ (with I_D in mA)

Next, assume the transistor is in saturation:

$$I_D = \frac{1}{2} k_n v_{OV}^2 = 0.5(V_{GS} - V_{tn})^2 = 0.5(5 - 6I_D - 1)^2$$

$18I_D^2 - 25I_D + 8 = 0$ --> $I_D = 0.89$mA or 0.5mA

If $I_D = 0.89mA$, $V_{GS} = -0.34V$, NMOS will be cut-off

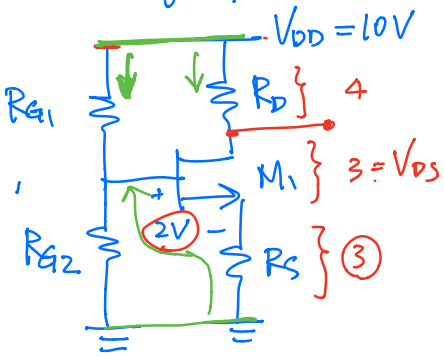
--> not a physical solution.

If $I_D = 0.5$mA, $V_{GS} = 2V$, $V_{OV} = 2 - 1 = 1V$

$V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 6 = 4V > V_{OV}$

Saturation assumption verified !

As a design problem



$V_{OV}=V_{GS}-V_{t,n}$

$V_{GS}=V_{OV}+V_{t,n}$

NMOS. $V_{t,n}=1V$, $k_n=1mA/V^2$

Design goal $I_D=0.5mA$

Assume M_1 is saturation

$I_D=\frac{1}{2}k_n V_{OV}^2=0.5mA$ ⟸

$k_n = 1mA/V^2$

$V_{OV}^2=1 \Rightarrow V_{OV}=1V$

$V_{GS}=V_{OV}+V_{t,n}=1+1=2V$

Design rule of thumb:

≈ 1/3 voltage drop to each element

$V_{DS}=3V \longrightarrow > V_{OV}=1V$

verify M_1 is indeed in saturation

$R_D=\frac{4V}{0.5mA}=8k\Omega$

$R_S=\frac{3V}{0.5mA}=6k\Omega$

$V_G=3+2=5V$

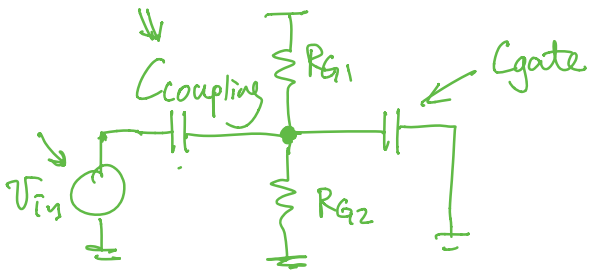
$R_{G1}=R_{G2}$, $V_G=\frac{R_{G2}V_{DD}}{R_{G1}+R_{G2}}=5V$ ✓

What do we choose $R_{G1}=R_{G2}=?$

① Choose large R_G to minimize power consumption

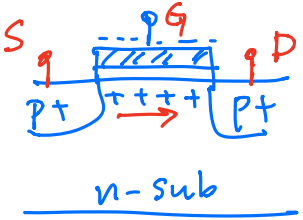
② eg. $R_{G1}=R_{G2}=1M\Omega$ or $10M\Omega$

Choose

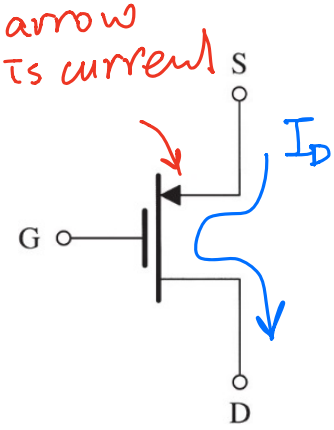


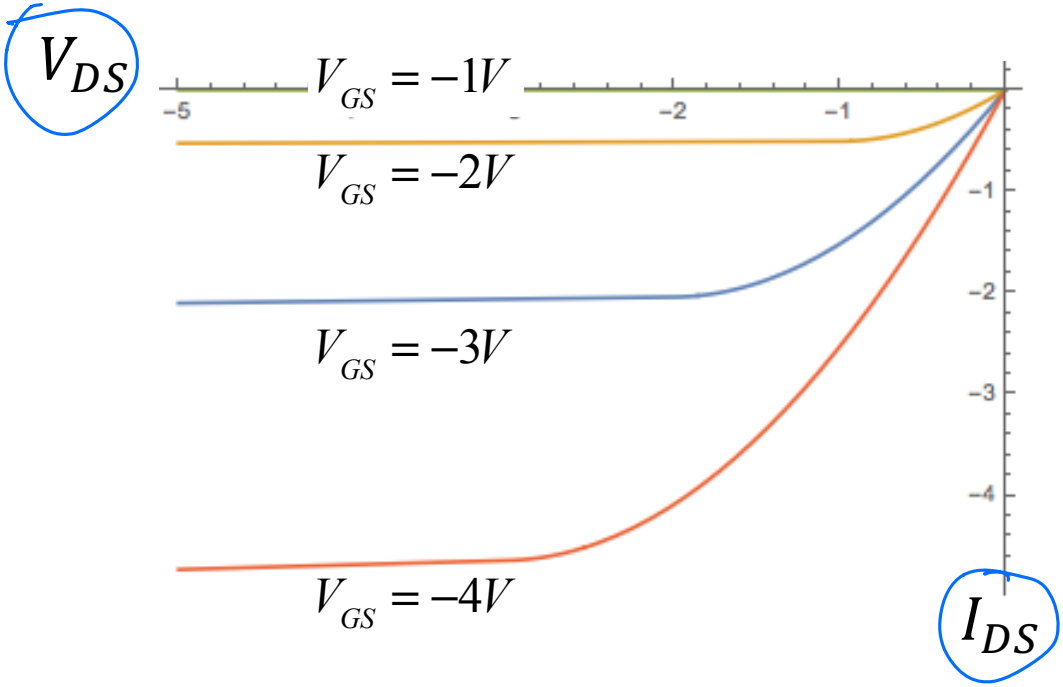
RC time

⇒ Bandwidth

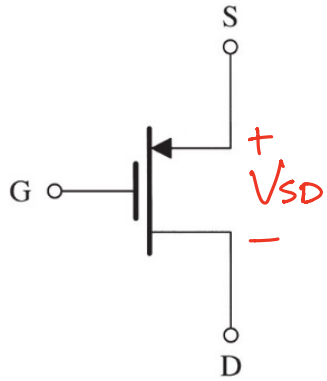


PMOS I-V Curves

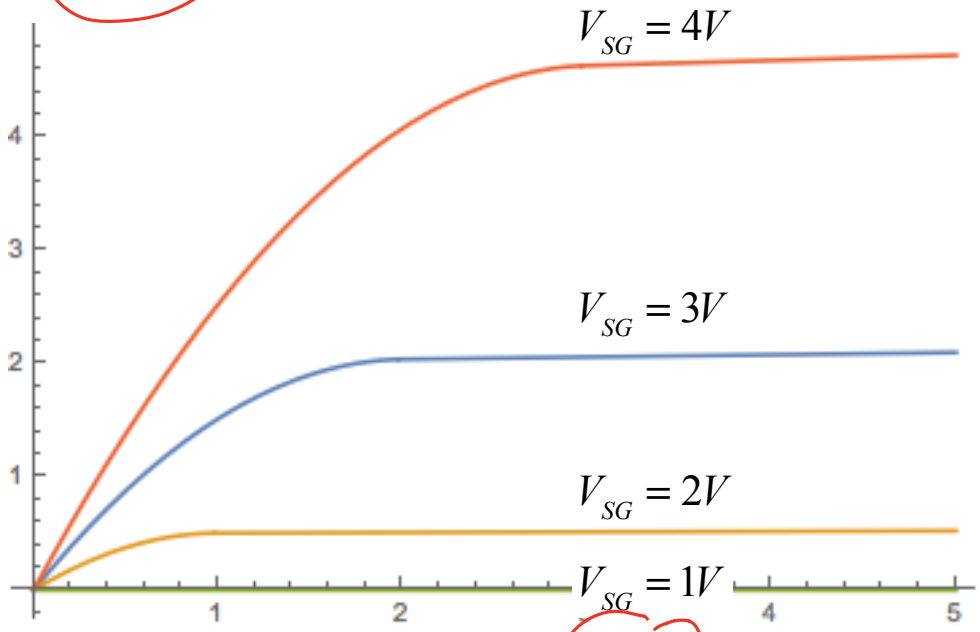




Right Side Up!

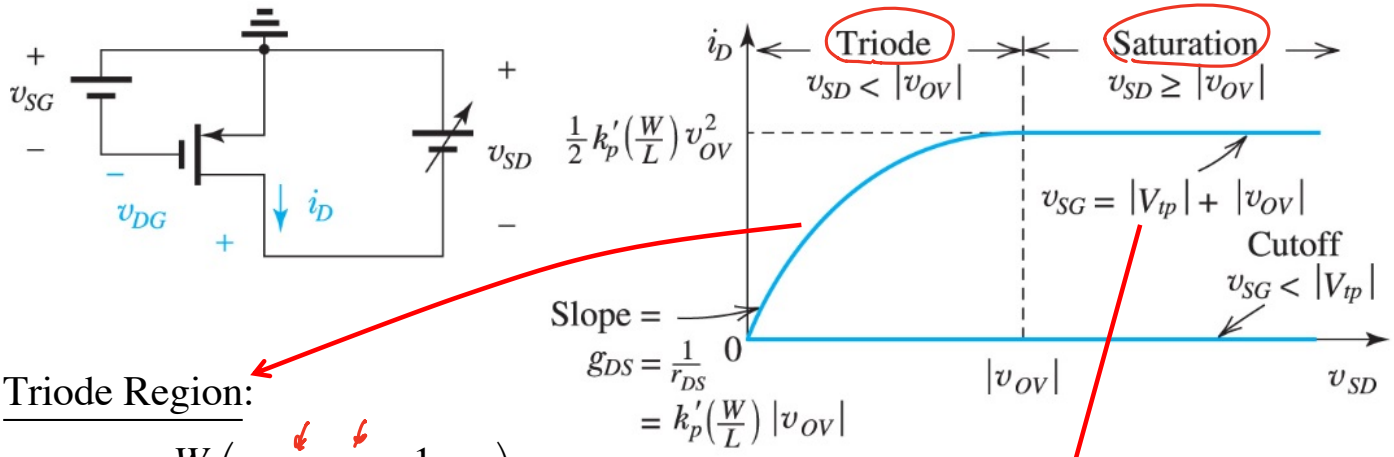


$$I_{SD} = |I_{DS}|$$



$$V_{SD} = |V_{DS}|$$

PMOS I-V Equations



Triode Region:

$$i_D = \mu_p C_{ox}\frac{W}{L}\left(|v_{OV}||v_{DS}| - \frac{1}{2}v_{DS}^2\right)$$

$$v_{OV} = |v_{SG}| - |V_{tp}|$$

Use same equation as NMOS but add absolute sign on all voltages since most voltages are negative:

$V_{tp} < 0,\ v_{DS} < 0,\ v_{GS} < 0$

So either use v_{SD} or $|v_{DS}|$

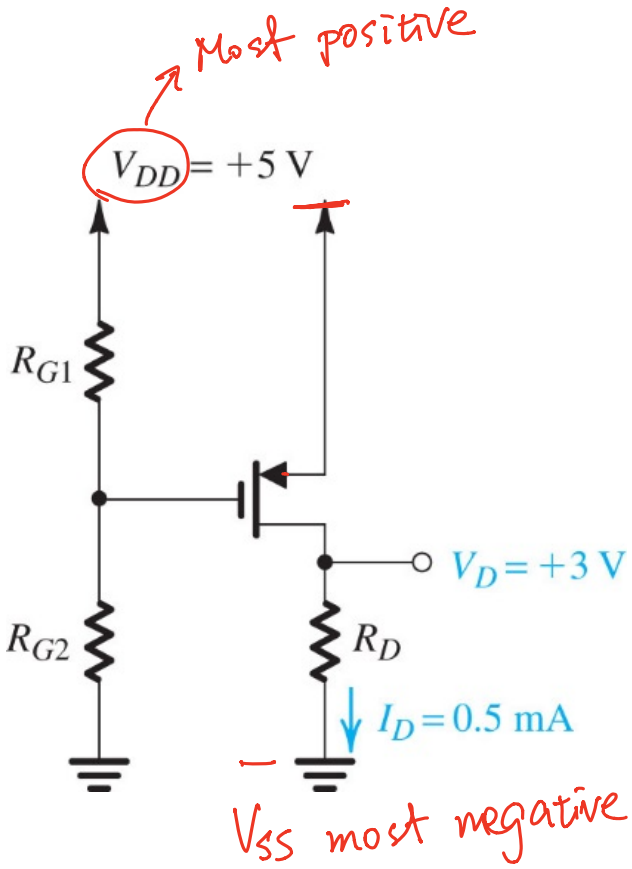
Saturation Region:

$$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(|v_{GS}| - |V_{tp}|\right)^2$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)v_{OV}^2$$

k_p

Example Circuit (3)



Design Problem:

Design the circuit such that $I_D = 0.5mA$ and $V_D = 3V$.

PMOS has $V_{tp} = -1V$, $\mu_p C_{ox}(W/L) = 1mA/V^2$.

Also find the maximum R_D for PMOS to remain in Saturation

Solution:

$$I_D = \frac{1}{2}k_p V_{OV}^2 = 0.5mA \quad \text{--->} \quad |V_{OV}| = 1V$$

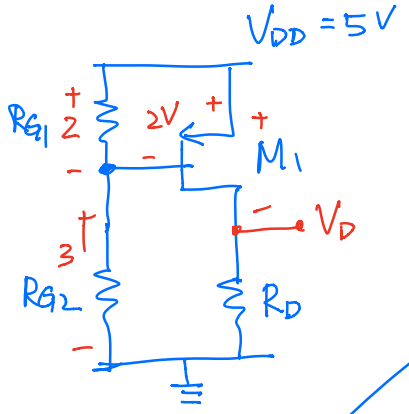
$$|V_{GS}| = |V_{tp}| + |V_{OV}| = 1 + 1 = 2V$$

$V_S = 5V$ --> $V_G = 3V$

We can choose $R_{G1} = 2M\Omega$ and $R_{G2} = 3M\Omega$

Saturation: $V_D \le 5 - |V_{OV}| = 4V$

$$R_{D,\max} = \frac{V_{D,\max}}{I_D} = \frac{4}{0.5} = 8k\Omega$$



Design example

PMOS: $V_{tp}=-1V$, $k_p=1mA/V^2$

Design goal $I_D=0.5V$

M_1 in saturation

$$I_D=\frac{1}{2}k_p V_{ov}^2=0.5\,mA$$

(k_p: $1mA/V^2$)

$$\Rightarrow V_{ov}^2=1V \Rightarrow |V_{ov}|=1$$

$$|V_{GS}|=|V_{ov}|+|V_{t,p}|=1+1=2V$$

Choose $V_D=\frac{1}{2}V_{DD}=2.5V$

$$\Rightarrow |V_{DS}|=|V_{DD}-V_D|=2.5V>|V_{ov}| \checkmark$$

M_1 indeed in saturation

R_{G1}, R_{G2},

Choose $R_{G1}=2M\Omega$, $R_{G2}=3M\Omega$

$$V_G=V_{DD}\cdot\frac{R_{G2}}{R_{G1}+R_{G2}}=3V$$

Consider channel length modulation

$$\frac{1}{2}k_p V_{ov}^2(1+\lambda|V_{DS}|)=0.5mA$$

$\Rightarrow$ Solving Bias (DC) Problem by hand, Ignore λ

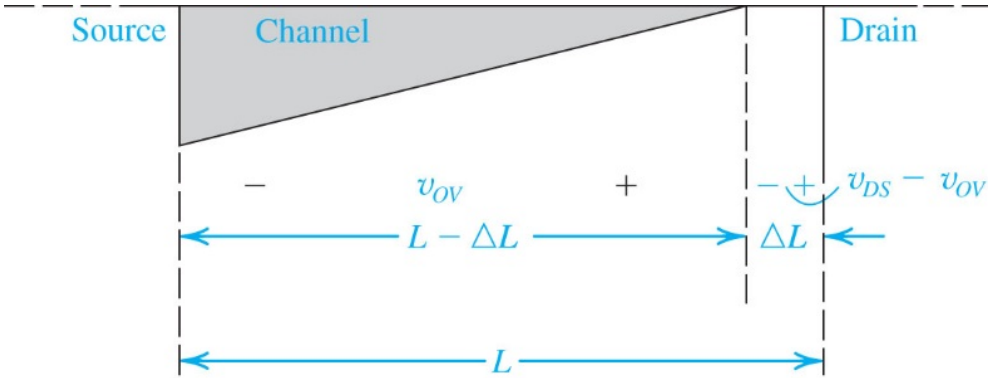
Finite Output Resistance due to Channel Length Modulation

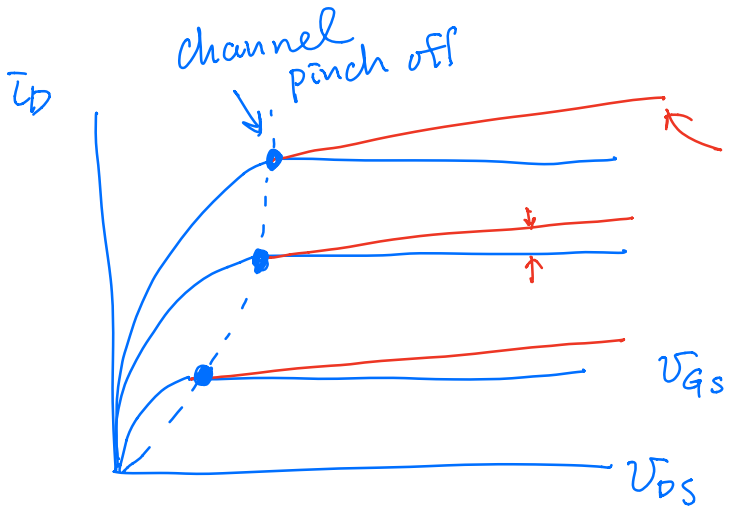
When $v_{DS} = v_{OV}$, the channel pinch of near the Drain. With further increase in v_{DS}, the pinch off point moves slowly towards the source, effectively reducing the channel length from L to $L - \Delta L$ (this is called "channel length modulation"):

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L-\Delta L}\left(v_{GS} - V_{tn}\right)^2$$

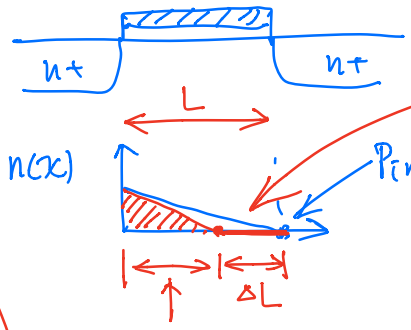
The continual increase of i_D with v_{DS} is modeled by

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS} - V_{tn}\right)^2\left(1 + \lambda v_{DS}\right)$$





$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\cdot V_{OV}^2$ indep of V_{DS}



Channel length modulation

$V_{DS} = V_{OV} = V_{GS} - V_{tn}$

Increase V_{DS} further

$L_{eff} = L - \Delta L$ $\quad \boxed{\Delta L \propto V_{DS}}$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L-\Delta L}\right)\cdot V_{OV}^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2\cdot\left(\frac{1}{1-\frac{\Delta L}{L}}\right)$$

$\frac{\Delta L}{L} \ll 1$ $\quad \left(1-\frac{\Delta L}{L}\right)^{-1} \approx 1+\frac{\Delta L}{L} = \lambda V_{DS}$ $\quad \frac{1}{1-\epsilon} \approx 1+\epsilon$

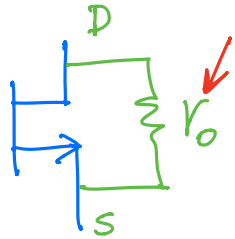
Consider channel length modulation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\cdot V_{OV}^2\,(1+\lambda V_{DS})$$

Output Resistance of MOSFET

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_{tn})^2(1+\lambda v_{DS})$$

$$r_o = \left(\frac{\partial v_{DS}}{\partial i_D}\right)_{v_{GS}=V_{GS}} = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}_{v_{GS}=V_{GS}} = \frac{1}{\lambda\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2\right)} \approx \frac{1}{\lambda I_D}$$



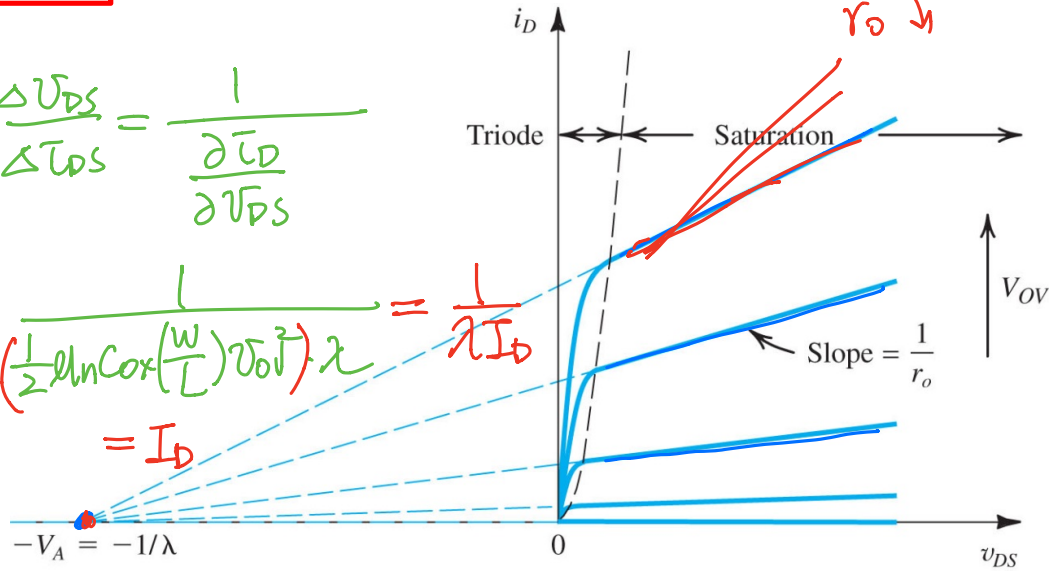
$r_o = r_{ds}$

$$r_o = \frac{1}{\lambda I_D}$$ where $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2$ is the DC bias current at Drain.

$r_o = \frac{\Delta v_{DS}}{\Delta i_D} = \frac{1}{\frac{\partial i_D}{\partial v_{DS}}}$

$= \frac{1}{\left(\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)v_{OV}^2\right)\lambda} = \frac{1}{\lambda I_D}$

$= I_D$



r_o ↘

Ignore λ ($\lambda = 0$)

$r_o = \frac{1}{\lambda I_D} \to \infty$

Fine for DC

For AC consider λ

To find V_A

$$I_D = 0 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2\left[1+\lambda(-V_A)\right]$$

$$\Rightarrow 1-\lambda V_A = 0 \Rightarrow V_A = \frac{1}{\lambda}$$ ("Early" Voltage)

λ : $[V^{-1}]$

↑ Name derive from BJT terminology